CMOS FABRICATED ON DIFFERENT CRYSTALLOGRAPHIC ORIENTATION SUBSTRATES

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BACKGROUND

[0001] The present disclosure relates generally to microelectronic devices and, more specifically, to a microelectronic device fabricated on substrates having different crystallographic orientations, a method of manufacture therefor, and an integrated circuit incorporating the same.

[0002] One transistor performance parameter of frequent discussion is electron mobility. This parameter is a measure of electron scattering in a semiconductor material, relating the proportionality between electron drift velocity and electric field as well as carrier concentration and conductivity of the semiconductor. Drift velocity relates the velocity of carriers under an electric field. That is, in contrast to carriers in free space, carriers in a semiconductor are not "infinitely" accelerated by an electric field due to scattering. Accordingly, carriers in a semiconductor reach a finite velocity regardless of the period of time over which the field is acting. At a given electric field, drift velocity is determined by the carrier mobility. Generally, increasing electron mobility provides an increase in performance of negative-biased transistors.

[0003] Another transistor performance parameter is hole mobility. This parameter is a measure of hole scattering in a semiconductor, relating the proportionality between hole drift velocity and electric field as well as conductivity and hole concentration in the semiconductor. Due to the higher effective mass of a hole, hole mobility is typically significantly lower than

electron mobility. Generally, increasing hole mobility provides an increase in performance of positive-biased transistors.

[0004] According to some industry reports, electron mobility is maximized when employing substrates having a (1,0,0) crystalline orientation, and hole mobility is maximized when employing substrates having a (1,1,0) crystalline orientation. Thus, microelectronic devices employing positive-biased transistors are often formed on substrates having a (1,1,0) crystalline orientation, whereas microelectronic devices employing negative-biased transistors are often formed on substrates having a (1,0,0) crystalline orientation. However, for microelectronic devices employing complimentary transistor configurations in which neighboring pairs of transistors include one negative-biased transistor and one positive-biased device (e.g., CMOS devices), single-crystalline-orientation substrates achieve only one of increased hole mobility and increase electron mobility, because microelectronic device substrate (e.g., silicon wafers) generally have only one crystalline orientation.

[0005] Accordingly, what is needed in the art is a device and method of manufacture thereof that addresses the above-discussed issues.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0007] Fig. 1A illustrates a sectional view of one embodiment of a microelectronic device in an intermediate stage of manufacture according to aspects of the present disclosure.

[0008] Fig. 1B illustrates a sectional view of the microelectronic device shown in Fig. 1A in a subsequent stage of manufacture.

[0009] Fig. 1C illustrates a sectional view of the microelectronic device shown in Fig. 1B in a subsequent stage of manufacture.

[0010] Fig. 1D illustrates a sectional view of the microelectronic device shown in Fig. 1C in a subsequent stage of manufacture.

[0011] Fig. 2A illustrates a sectional view of another embodiment of a microelectronic device in an intermediate stage of manufacture according to aspects of the present disclosure.

[0012] Fig. 2B illustrates a sectional view of the microelectronic device shown in Fig. 2A in a subsequent stage of manufacture.

[0013] Fig. 2C illustrates a sectional view of the microelectronic device shown in Fig. 2B in a subsequent stage of manufacture.

[0014] Fig. 2D illustrates a sectional view of the microelectronic device shown in Fig. 2C in a subsequent stage of manufacture.

[0015] Fig. 3A illustrates a sectional view of another embodiment of a microelectronic device in an intermediate stage of manufacture according to aspects of the present disclosure.

[0016] Fig. 3B illustrates a sectional view of the microelectronic device shown in Fig. 3A in a subsequent stage of manufacture.

[0017] Fig. 3C illustrates a sectional view of the microelectronic device shown in Fig. 3B in a subsequent stage of manufacture.

[0018] Fig. 3D illustrates a sectional view of the microelectronic device shown in Fig. 3C in a subsequent stage of manufacture.

[0019] Fig. 4 illustrates a sectional view of one embodiment of an integrated circuit device constructed according to aspects of the present disclosure.

DETAILED DESCRIPTION

[0020] It is to be understood that the following disclosure provides many different embodiments, or examples, for implementing different features of various embodiments. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed. Moreover, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed interposing the first and second features, such that the first and second features may not be in direct contact.

[0021] Referring to Fig. 1A, illustrated is a sectional view of one embodiment of a microelectronic device 100 in an intermediate stage of manufacture according to aspects of the present disclosure. The microelectronic device 100 includes a substrate 110 and a substrate 120.

[0022] The substrates 110, 120 may each comprise an elementary semiconductor (such as crystal silicon, polycrystalline silicon, amorphous silicon and germanium), a compound semiconductor (such as silicon carbide and gallium arsenide), an alloy semiconductor (such as silicon germanium, gallium arsenide phosphide, aluminum indium arsenide, aluminum gallium arsenide and gallium indium phosphide), combinations thereof and/or other materials. The substrates 110, 120 may also each comprise a semiconductor material on an insulator, such as a silicon-on-insulator (SOI) substrate, a silicon on sapphire (SOS) substrate, or a thin film transistor (TFT). In one embodiment, the substrates 110, 120 may also each include a doped epitaxial layer. The substrates 110, 120 may also each include a multiple silicon structure or a multilayer, compound semiconductor structure.

[0023] The substrates 110, 120 are bonded or otherwise coupled together. Such coupling may employ wafer bonding utilizing mirror-polished, flat and clean wafers. When two wafers are brought into contact, they may be locally attracted to each other by Van der Waals forces and thereby and thereafter bonded to each other. The wafer bonding process may be initiated by

locally applying a slight pressure to the wafer pair, such that the bonded area may spread laterally over a substantial portion of the wafer contact area in a few seconds. In some embodiments, bonded wafer pairs may be exposed to a heat treatment to strengthen the bonding interface.

[0024] The substrates 110, 120 have different crystallographic orientations. For example, the substrate 110 may have a (1,1,0) crystallographic orientation and the substrate 120 may have a (1,0,0) crystallographic orientation. In another embodiment, the substrate 110 may have a (1,0,0) crystallographic orientation and the substrate 120 may have a (1,1,0) crystallographic orientation. Of course, the substrates 110, 120 may have crystallographic orientations other than those described above. In one embodiment, the different crystallographic orientations of the substrates 110, 120 may only be in adjacent portions of the substrates 110, 120. For example, the substrate 110 may comprise a layer that is adjacent a layer of the substrate 120, wherein the two adjacent layers have different crystallographic orientations, although the bulk portions of the substrates 110, 120 may have similar or other crystallographic orientations.

[0025] Referring to Fig. 1B, illustrated is a sectional view of the microelectronic device 100 shown in Fig. 1A in a subsequent stage of manufacture, in which a portion of the substrate 120 has been removed to expose a portion of the substrate 110. Such removal of a portion or portions of the substrate 120 may form one or more openings in the substrate 120 exposing the substrate 110. For example, one or more dry and/or wet etching processes may be employed to pattern the substrate 120. The etching process may comprise an isotropic etch, in which the rate of etching reaction is significant in more than one direction, or an anisotropic etch, which the rate of etching is more substantial in one or more predetermined directions than in other directions. The etching process may also employ photolithographic and/or masking process in which a portion of the substrate 120 is shielded from an etching composition.

[0026] As also shown, a dielectric film 130 may be formed over the second substrate 120 after the second substrate 120 has been patterned. The dielectric film 130 may be blanket deposited or otherwise conformally formed over the second substrate 120 such that the dielectric film 130 also substantially spans a sidewall 125 of the substrate 120 defined during the prior patterning processing.

[0027] The dielectric film 130 may be formed over the substrate 120 by thermal oxidation, atomic layer deposition (ALD), chemical vapor deposition (CVD), plasma-enhanced CVD (PECVD), physical vapor deposition (PVD), and/or other processes. Moreover, although not limited by the scope of the present disclosure, the dielectric film 130 may comprise oxide, silicon oxide, silicon nitride, silicon oxynitride, hafnium oxide, zirconium oxide, aluminum oxide, a hafnium dioxide-alumina (HfO_2–Al_2O_3) alloy, combinations thereof and/or other materials. A masking process may be employed to prevent formation of the dielectric film 130 on the substrate 110, or the deposition of the dielectric film 130 may be a selective deposition. An etching or other material removal process or a masking process may also be employed to remove any portion of the dielectric film 130 formed on the substrate 110. The dielectric film 130 may have a thickness ranging between about 5 Angstroms and about 100 Angstroms. Although not shown in the illustrated embodiment, one or more seed layers, adhesion layers, and/or diffusion barrier layers may also be formed between the dielectric film 130 and the substrate 120 and/or over the dielectric film 130.

[0028] Referring to Fig. 1C, illustrated is a sectional view of the semiconductor device 100 shown in Fig. 1B in a subsequent stage of manufacture, in which an extension 140 of the first substrate 110 has been formed in the void created by the patterning processing of the second substrate 120 described above. In one embodiment, the extension 140 may be epitaxially grown, such as by a selective epitaxial growth (SEG). The extension 140 may have a crystallographic orientation that is substantially similar or identical to the crystallographic orientation of the substrate 110 and different from the crystallographic orientation of the substrate 120. For example, the extension 140 and the substrate 110 may have a (1,1,0) crystallographic orientation and the substrate 120 may have a (1,0,0) crystallographic orientation. In another embodiment, the extension 140 and the substrate 110 may have a (1,0,0) crystallographic orientation and the substrate 120 may have a (1,1,0) crystallographic orientation. Chemical-mechanical polishing or chemical-mechanical planarizing (collectively referred to herein as CMP) may be employed to planarize the extension 140, such that the extension 140 may be substantially coplanar with the dielectric film 130.

[0029] Referring to Fig. 1D, illustrated is a sectional view of the semiconductor device 100 shown in Fig. 1C in a substrate stage of manufacture, in which semiconductor devices 150, 160

have been formed. The semiconductor devices 150, 160 may be or comprise metal-oxide-semiconductor field-effect-transistors (MOSFETs), Fin-FETs, memory cells, and/or other conventional or future-developed semiconductor devices. In one embodiment, the semiconductor devices 150, 160 may each be or comprise complimentary metal-oxide-semiconductor (CMOS) devices, such that one of the semiconductor devices 150, 160 may be or comprise an n-type transistor and the other of the semiconductor devices 150, 160 may be or comprise a p-type transistor. One or more CMP processes may be employed prior to forming the semiconductor devices 150, 160 such that the substrate 120, the dielectric film 130, and the extension 140 may collectively form a substantially coplanar surface on which the semiconductor devices 150, 160 may be formed.

[0030] Referring to Fig. 2A, illustrated is a sectional view of another embodiment of a microelectronic device 200 in an intermediate stage of manufacture according to aspects of the present disclosure. The microelectronic device 200 may be substantially similar to the microelectronic device 100 shown in Figs. 1A-1D. For example, the microelectronic device 200 includes coupled substrates 110, 120 which may be substantially similar to those shown in Figs. 1A-1D.

[0031] Referring to Fig. 2B, illustrated is a sectional view of the microelectronic device 200 shown in Fig. 2A in a subsequent stage of manufacture. The microelectronic device 200 also includes an isolation structure 210 substantially spanning the thickness of the substrate 120 and extending at least partially into the substrate 110. The isolation structure 210 may also extend substantially through the substrate 110. In one embodiment, the isolation structure 210 is a shallow trench isolation (STI) element. The isolation structure 210 may be formed by etching or otherwise patterning a recess extending substantially through the substrate 120 and partially into the substrate 110. The recess may be filled with a bulk dielectric material, possibly after a diffusion barrier layer is deposited to line the recess. Of course, other isolation structures and methods of manufacture thereof are within the scope of the present disclosure.

[0032] Referring to Fig. 2C, illustrated is a sectional view of the microelectronic device 200 shown in Fig. 2B in a subsequent stage of manufacture, in which a portion of the substrate 120

has been removed or the substrate 120 has been otherwise patterned. The substrate 120 may be patterned by processes similar to those discussed above with reference to Fig. 1B.

[0033] Referring to Fig. 2D, illustrated is a sectional view of the microelectronic device 200 shown in Fig. 2C in a subsequent stage of manufacture, in which an extension 140 has been formed from the substrate 110 and adjacent the substrate 120. The extension 140 may be formed by processes similar to those discussed above with reference to Fig. 1C. Fig. 2D also illustrates the formation of semiconductor devices 150, 160 over the substrate 120 and the extension 140, respectively. The semiconductor devices 150, 160 and their manufacture may be substantially similar to those discussed above with reference to Fig. 1D.

[0034] Referring to Fig. 3A, illustrated is a sectional view of another embodiment of a microelectronic device 300 in an intermediate stage of manufacture according to aspects of the present disclosure. The microelectronic device 300 may be substantially similar to the microelectronic device 100 shown in Figs. 1A-1D. For example, the microelectronic device 300 includes coupled substrates 110, 120 which may be substantially similar to those shown in Figs. 1A-1D.

[0035] However, the microelectronic device 300 also includes an insulator layer 310 interposing the substrates 110, 120. The insulator layer 310 may be formed over the substrate 110 by thermal oxidation, ALD, CVD, PECVD, PVD, and/or other processes. The insulator layer 310 may also be or comprise a buried oxide layer, such as that formed by implanting oxide and/or another insulator material through at least a portion of the substrate 120. Although not limited by the scope of the present disclosure, the insulator layer 310 may comprise oxide, silicon oxide, silicon nitride, silicon oxynitride, hafnium oxide, zirconium oxide, aluminum oxide, a hafnium dioxide-alumina (HfO_2–Al_2O_3) alloy, combinations thereof and/or other materials. The insulator layer 310 may have a thickness ranging between about 5 Angstroms and about 100 Angstroms. Although not shown in the illustrated embodiment, one or more seed layers, adhesion layers, and/or diffusion barrier layers may also be formed between the insulator layer 310 and the substrate 110 and/or over the insulator layer 310.

[0036] Referring to Fig. 3B, illustrated is a sectional view of the microelectronic device 300 shown in Fig. 3A in a subsequent stage of manufacture, in which a portion of the substrate 120

and the insulator layer 310 have been removed to expose a portion of the substrate 110. For example, one or more dry and/or wet etching processes may be employed to pattern the substrate 120. The etching process may comprise an isotropic etch, in which the rate of etching reaction is significant in more than one direction, or an anisotropic etch, which the rate of etching is more substantial in one or more predetermined directions than in other directions. The etching process may also employ a mask or masking process, thereby shielding a portion of the substrate 120 from the etching process.

[0037] As also shown, a dielectric film 130 may be formed over the second substrate 120 after the second substrate 120 has been patterned. The dielectric film 130 may be blanket deposited or otherwise conformally formed over the second substrate 120 such that the dielectric film 130 also substantially spans the insulator layer 310 and a sidewall 125 of the substrate 120 defined during the prior patterning processing.

[0038] The dielectric film 130 may be formed over the substrate 120 by thermal oxidation, ALD, CVD, PECVD, PVD, and/or other processes. Although not limited by the scope of the present disclosure, the dielectric film 130 may comprise oxide, silicon oxide, silicon nitride, silicon oxynitride, hafnium oxide, zirconium oxide, aluminum oxide, a hafnium dioxide-alumina (HfO_2–Al_2O_3) alloy, combinations thereof and/or other materials. A masking process may be employed to prevent formation of the dielectric film 130 on the substrate 110, or the deposition of the dielectric film 130 may be a selective deposition. An etching or other material removal process or a masking process may also be employed to remove any portion of the dielectric film 130 formed on the substrate 110. The dielectric film 130 may have a thickness ranging between about 5 Angstroms and about 100 Angstroms. Although not shown in the illustrated embodiment, one or more seed layers, adhesion layers, and/or diffusion barrier layers may also be formed between the dielectric film 130 and the substrate 120 and/or over the dielectric film 130.

[0039] Referring to Fig. 3C, illustrated is a sectional view of the semiconductor device 300 shown in Fig. 3B in a subsequent stage of manufacture, in which an extension 140 of the first substrate 110 has been formed in the void created by the patterning processing of the second substrate 120 described above. In one embodiment, the extension 140 may be epitaxially grown,

such as by a selective epitaxial growth (SEG). The extension 140 may have a crystallographic orientation that is substantially similar or identical to the crystallographic orientation of the substrate 110 and different from the crystallographic orientation of the substrate 120. For example, the extension 140 and the substrate 110 may have a (1,1,0) crystallographic orientation and the substrate 120 may have a (1,0,0) crystallographic orientation. In another embodiment, the extension 140 and the substrate 110 may have a (1,0,0) crystallographic orientation and the substrate 120 may have a (1,1,0) crystallographic orientation. Chemical-mechanical polishing or chemical-mechanical planarizing (collectively referred to herein as CMP) may be employed to planarize the extension 140, such that the extension 140 may be substantially coplanar with the dielectric film 130.

[0040] Referring to Fig. 3D, illustrated is a sectional view of the microelectronic device 300 shown in Fig. 3C in a subsequent stage of manufacture, in which semiconductor devices 150, 160 have been formed over the substrate 120 and the extension 140, respectively. The semiconductor devices 150, 160 and their manufacture may be substantially similar to those discussed above with reference to Fig. 1D.

[0041] As also shown, a portion of the dielectric film 130 may be removed prior to forming the semiconductor devices 150, 160. For example, etching and/or CMP may be employed to remove the portion of the dielectric film 130 that is opposite the substrate 120 from the substrate 110, thereby exposing the substrate 120. Such processing may also be employed to remove a portion of the extension 140 such that the extension and the substrate 120 are substantially coplanar. However, the portion of the dielectric film 130 interposing the substrate 120 and the extension 140 may remain to electrically isolate the substrate 120 from the extension 140.

[0042] Referring to Fig. 4, illustrated is a sectional view of one embodiment of an integrated circuit device 400 constructed according to aspects of the present disclosure. The integrated circuit device 400 is one environment in which aspects of the above-described microelectronic devices may be implemented. For example, the integrated circuit device 400 includes a plurality of microelectronic devices 410 located on and/or in a substrate 430, one or more of which may be substantially similar to one or more of the microelectronic devices 100, 200, and 300 shown in Figs. 1D, 2D, and 3D, respectively. The microelectronic devices 410 may be interconnected,

and may be connected to one or more MOSFETs, Fin-FETs, memory cells, and/or other conventional or future-developed semiconductor devices manufactured on and/or in the substrate 430.

[0043] The integrated circuit device 400 also includes interconnects 440 extending along and/or through one or more dielectric layers 450 to ones of the plurality of microelectronic devices 410. The dielectric layers 450 may comprise silicon dioxide, Black Diamond® (a product by Applied Materials of Santa Clara, California) and/or other materials, and may be formed by CVD, PECVD, ALD, PVD, spin-on coating and/or other processes. The dielectric layers 450 may have a thickness ranging between about 2000 Angstroms and about 15,000 Angstroms. The interconnects 440 may comprise copper, tungsten, gold, aluminum, carbon nano-tubes, carbon fullerenes, refractory metals, and/or other materials, and may be formed by CVD, ALD, PVD and/or other processes.

[0044] Thus, the present disclosure introduces a microelectronic device including, in one embodiment, a microelectronic device including a first substrate bonded to a second substrate. The first substrate includes an opening through which an epitaxially grown portion of the second substrate extends. A first semiconductor device is coupled to the first substrate, and a second semiconductor device is coupled to the epitaxially grown portion of the second substrate. In one embodiment, the first and second substrates have different crystallographic orientations.

[0045] The present disclosure also provides a method of manufacturing a microelectronic device. In one embodiment, the method includes coupling a first substrate to a second substrate and patterning an opening in the first substrate. The first and second substrates may have different crystallographic orientations. An extension of the second substrate is epitaxially grown through the opening. A first semiconductor device is formed on the first substrate, and a second semiconductor device is formed on the extension of the second substrate.

[0046] The present disclosure also provides an integrated circuit device. In one embodiment, the integrated circuit device includes a first substrate having a plurality of openings extending therethrough, and a second substrate coupled to the first substrate and including a plurality of epitaxially grown extensions each extending through a corresponding one of the plurality of openings. A plurality of first semiconductor devices are each coupled to the first substrate. A

plurality of second semiconductor devices are each coupled to a corresponding one of the plurality of extensions.

[0047] The foregoing has outlined features of several embodiments so that those skilled in the art may better understand the detailed description that follows. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions and alterations herein without departing from the spirit and scope of the present disclosure.